Relaxation into Tunnel Induced Non-equilibrium States in Metal Oxide Semiconductor Structures

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The relaxation of a Metal Oxide Semiconductor structure from deep depletion towards a tunnel induced non-equilibrium stationary state is addressed in this work. A simple model was constructed, taking into account thermal generation, tunneling of both types of carriers and impact ionization. Experimental results obtained on *p*- and *n*-type Si substrates and oxides thinner than 6.5 nm are shown to be well fitted by the proposed model. A map describing the possible behavior patterns for a structure with given oxide thickness and effective generation velocity is presented.

The transients in an Metal Oxide Semiconductor (MOS) structure relaxing from deep depletion towards equilibrium were previously investigated in connection with the characterization of the minority carriers generation mechanisms. It is assumed, for the methods to be applicable, that the transient ends in the thermal equilibrium state. The presence of tunneling currents alters this behavior, affecting the transient to yield a steady state different from thermal equilibrium [1–5].

Very thin oxide samples exhibit similar transients for both *p*- and *n*-type substrates. This symmetry breaks down for oxide thicknesses above 3.5 nm. Three qualitatively different behavior patterns, depending of the oxide thickness, can be identified through current transient curves for the *n*-type substrate samples. From the analysis of the associated currents, the three patterns correspond to i) *p*-type substrate samples and very thin oxide *n*-samples for which minority carriers seem to dominate the tunneling current, ii) intermediate oxide thickness (3–6 nm) on *n*-substrates, for which the tunneling current is dominated by majority carriers but the whole current is limited by the generation of minority carriers, and iii) thicker oxides on *n*-substrates, for which the impact ionization mechanism removes the limit imposed to the current by supplying minority carriers.

The problem of modeling the relaxation of a MOS structure from deep depletion into tunnel induced non-equilibrium states is addressed in this work.

An exact formulation of this problem requires the coupling Poisson equation, continuity equations for holes and electrons, and complete expressions for the pair generation process, tunneling and impact ionization. An integral treatment for the continuity equations, as used in this work, leads to a unique differential equation describing the evolution towards equilibrium.

The model was tested by reproducing experimental results in the three regimes, and was used to analyze the dependence of each type of behavior on the thickness and generation parameters.

A map for the relationship between oxide thickness and thermal to obtain a given behavior pattern is given.

1. Theory

The measured current in the external circuit after applying a reverse voltage step to an *n*-MOS diode is given by [5]

$$J_m = J_{disp} + J_{tp} + J_{tn} = J_g + \frac{dQ_{dep}}{dt} + J_{tn}, \qquad (1)$$

where J_{disp} is the displacements current due to changes in the charge distribution within the semiconductor, and J_{tp} and J_{tn} are the conduction currents which in this case correspond to tunneling currents for holes and electrons, respectively. J_g is the minority carrier generation current into the inversion layer, and Q_{dep} is the space charge in the depleted region.

Charge conservation in integral form, applied to the inversion layer, is expressed as follows:

$$\frac{dQ_{inv}}{dt} = J_g - J_{tp}, \qquad (2)$$

where Q_{inv} is the inversion layer charge. Using the conservation of the electric displacement vector, the inversion layer charge takes the form

$$Q_{inv} = \left|V_g - V_s\right| \frac{\varepsilon_{ox}}{d} - qNW, \qquad (3)$$

where V_g is the applied voltage, V_s is the semiconductor potential, d is the oxide thickness, ε_{ox} is the oxide dielectric permittivity, q is the electron charge, N is the dopant concentration, and W is the depletion region width. Using the known dependence of W on V_s, the variation of Q_{inv} with time in terms of variations of V_s results in

$$\frac{dQ_{inv}}{dt} = \left[\frac{\varepsilon_{ox}}{d} + \frac{\varepsilon_s}{W(V_s)}\right] \frac{dV_s}{dt}, \qquad (4)$$

where ε_s is the semiconductor dielectric permittivity. Replacing in eq. (2) we obtain the differential equation for V_s

$$\frac{dV_s}{dt} = \frac{J_g - J_{tp}}{\left[C_{ox} + \frac{\varepsilon_s}{W}\right]}. \qquad (5)$$

The total generation current is written as

$$J_g = qn_i\left(\frac{W}{2\tau_g} + S_i\right)\left[1 - \exp\left(\frac{V_g - \theta}{2kT}\right)\right] + qS_d\,(p_s^{eq} - p_s)\,, \quad (6)$$

where n_i is the intrinsic concentration, k is the Boltzmann constant, τ_g is the bulk generation lifetime, S_i is the value of the surface generation when the surface is inverted, and S_d is the generation velocity for the depleted surface, given by [6]:

$$S_d = S_0\,\frac{N}{(p_s + 2n_i)},$$

where S_0 is a constant parameter, θ is the difference between the metal Fermi level and the minority carrier quasi Fermi level, p_s is the surface minority carrier concentration, which in terms of V_s is

$$p_s = \frac{(V_g - V_s)^2}{2kT\varepsilon_s}\left(\frac{\varepsilon_{ox}}{d}\right)^2 - \frac{qN}{kT}\left(|V_s| - \frac{kT}{q}\right), \quad (7)$$

where p_s^{eq} is the equilibrium minority carrier concentration at the surface calculated from eq. (7) with $V_s = V_s^{eq}$, the equilibrium semiconductor voltage drop calculated in [4,7]. The number of pairs generated by impact in the space charge region for $V_{ox} > 1.7$ V, approximately, [8] ($V_{ox} = V_g - V_s$) is

$$J_{gi} = \alpha W J_{tn}, \quad (8)$$

where α is the number of ionized pairs per unit of distance and J_{tn} is the majority carrier tunneling current [9].

The extraction of minority carriers by tunneling was modeled with the following expression:

$$J_{tp} = \left(C_h\,\frac{p_s}{\alpha_h^2 N_\nu} + J_g\right)\exp(-2k_0 d)\exp(-\alpha_h q V_{ox}), \quad (9)$$

where C_h, α_h are numerical constants for the hole tunneling. Eq. (9) keeps the exponential dependence of the current on the oxide voltage drop reported for the direct tunneling regime [9]. The prefactor in this expression represents the total supply of carriers with velocity normal to the barrier. It is composed by carriers in the inversion layer with the first term proportional to p_s [10], and the carriers generated and driven to the surface, J_g.

2. Experimental Results Fitting

The transient currents of a pulsed MOS diode into depletion can be classified, as was shown in a recent work [5], in three different behavior patterns, as follows.

a) Dominance of the current by minority carrier tunneling.

b) Tunneling of both type of carriers, with the current llimited by the generation of minority carriers.

c) Tunneling of both type of carriers without limitation by the minority carrier generation which is enhanced by impactionization.

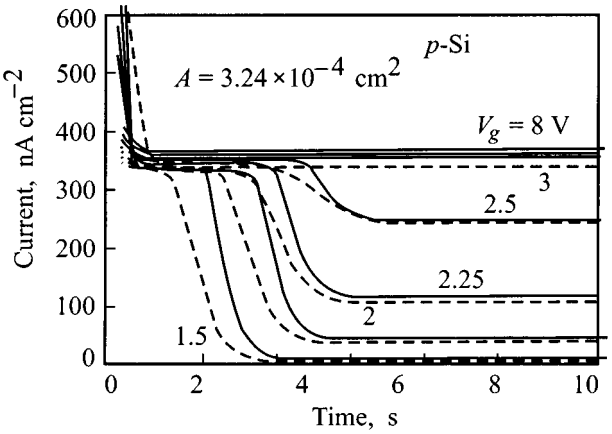

Figure 1. Experimental (solid) and calculated (dotted) curves, for a *p*-type sample, 4.5 nm oxide thickness, with different voltage pulses. *A* is the gate area.

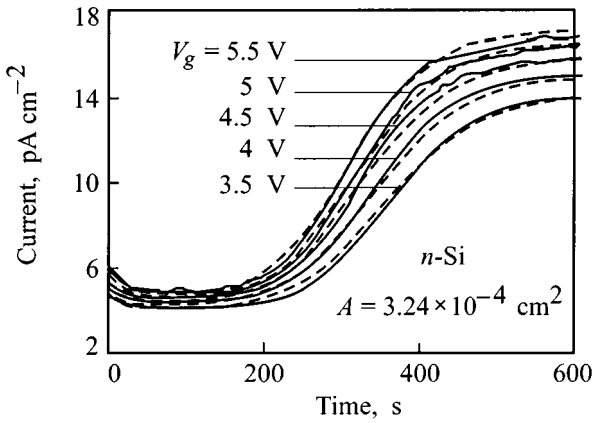

Figure 2. Experimental (solid) and calculated (dotted) curves, for an *n*-type sample, 3.7 nm oxide thickness.

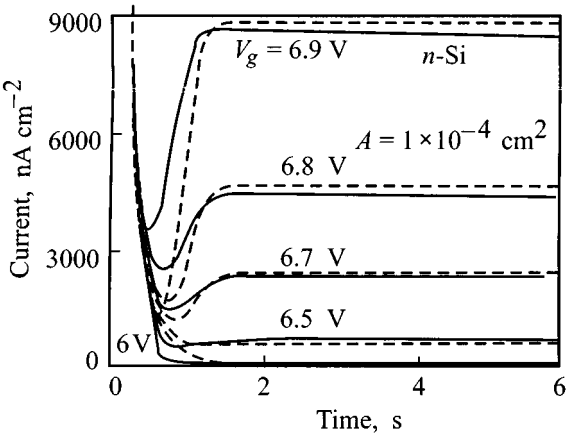

Figure 3. Experimental (solid) and calculated (dotted) curves, for an *n*-type sample, 6.3 nm oxide thickness.

Case a) is observed in the *p*-type substrate capacitors or in *n*-type with very thin insulators (up to about 3 nm). In *n*-samples with oxides between 3 and 6 nm, the impact ionization may occur but is insufficient for removing the generation limitation (case *b*). Case c) occurs for *n*-substrate samples with oxides thicker than about 6 nm.

Fig. 1 to 3 show a family of experimental curves pertaining to each one of the described cases fitted with the model proposed above. Details of the experimental work are given in ref. [5].

3. Discussion

In contrast to *p*-samples in which a unique kind of transient curve is measured, the behavior during the relaxation into tunnel induced non-equilibrium states in Metal Oxide Semiconductor structures with *n*-Si is determined by the oxide thickness and minority carrier generation parameters. The carrier generation can be characterized by an effective velocity, S_{eff}, as the total generation current density J_g divided qn_i. In the stationary state, the generation current should equal the hole tunnel current, J_{tp}. Thus, for the steady state the effective generation velocity is

$$S_{eff} = \frac{J_{tp}(V_{ox}, d)}{qn_i}. \tag{10}$$

A map for the different behaviors can be constructed plotting this velocity versus the oxide thickness (Fig. 4). This plot is divided into three regions. Structures laying in region I will exhibit curves like those shown in Fig. 1 for 3 and 8 V. No transient other than the decay of the surface generation velocity from its depleted value, S_0, to a stationary value, greater or equal to S_i can be measured on these diodes. Structures with parameters in region III, are those for which impact ionization spontaneously begins, enhancing generation of minority carriers (Fig. 3). Diodes between these two regions will show an increasing current transient (Fig. 2) due to the presence of a majority tunneling current without impactionization — region II.

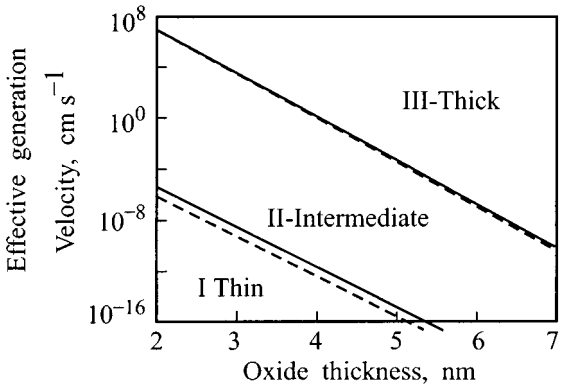

Figure 4. Behavior pattern map for MOS tunnel diodes with *n*-type substrate. The boundaries between regions were calculated for 3 V (solid line) and 50 V (dashed line) applied to the gate.

The boundaries between these regions, can be determined as follows. The condition to be fulfilled by a diode to lay in region III is that the stationary oxide voltage drop must be greater that the threshold for impact ionization, to ensure that impact ionization will begin during the evolution to equilibrium. Thus, from eq. (10) with $V_{ox} = 1.7$ V, the boundary between regions II and III is obtained. Diodes with higher S_{eff} or thicker oxide will exhibit the typical thick structure like behavior pattern.

Structures will be in region I if the surface is not inverted in the stationary state, so, the surface generation velocity will take a value between S_0 and S_i. Any tunneling current growth will be screened by the decreasing generation current. The minimum level of generation current before the inversion (or the maximum generation current when the surface is inverted) is obtained by replacing in the bulk generation expression the depletion width value immediately after the pulse, W_0, given by

$$W_0 = \frac{A\varepsilon_s}{C_{ox}}\left(\sqrt{1 - \frac{2V_g C_{ox}^2}{qN\varepsilon_s A^2}} - 1\right), \tag{11}$$

and then, the generation in this case will be

$$J_g = qn_i \frac{W_0}{2\tau_g} + qn_i S_i. \tag{12}$$

The initial oxide voltage in this situation is

$$V_{ox}^0 = V_g - \frac{qNW_0^2}{2\varepsilon_s}. \tag{13}$$

The prefactor in expression (9) for J_{tp}, i. e., the incident current, will be governed by J_g provided that the minority carrier concentration at the surface is too small. Replacing (9), (12) and (13) in eq. (10), the resulting S_{eff} vs. d curve represents the lowest boundary between regions I and II, i. e., diodes with smaller S_{eff} or d will exhibit a thin structure like behavior pattern.

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